

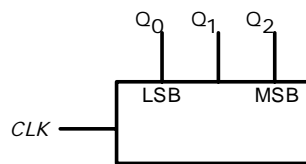
# DEVELOPMENT OF DIGITAL SYSTEMS

Examination  
07. 02. 2014

1. Draw a NAND only (Sheffer) implementation of a 4-bit prime number detector. The output of circuit is set to '1' whenever a 4-bit prime number is set on input (2, 3, 5, 7, 11, 13). Input numbers are represented by 4-bit Gray code. Calculate the COST function of resulting implementation.
2. Implement following functions using an imaginary "PAL3L3" circuit:
  - $f_1 = x_1 \oplus x_2$
  - $f_2 = x_1 \cdot x_2 \cdot x_3$
  - $f_3 = \text{majority function of three variables } x_1, x_2, x_3.$

A "PAL3L3" circuit is a PAL structure with 3 inputs and 3 outputs. Each OR term has 4 AND terms. Designation "L" signifies an inverted output. Mark programmed connections using dots on PAL3L3 schematic given on the **back side**.

3. Synthesize a 3 bit binary down counter using T type flip-flops: Draw the state transition table, determine T flip-flop input equations and draw the resulting counter circuit using signal names in the figure below.



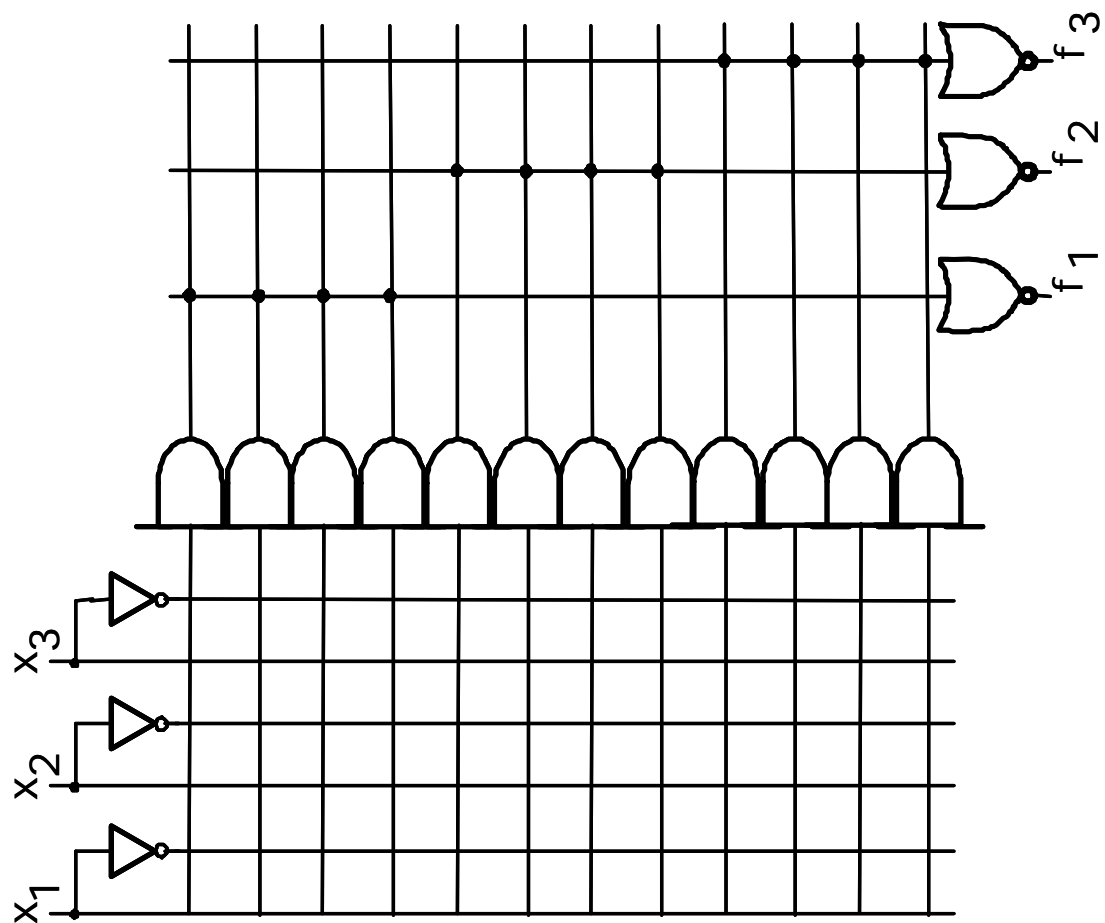
4. Draw a state diagram of a sequence detector FSM. Sequence detector has an input  $w$  and an output  $z$ . The FSM sets the output  $z='1'$ , when a sequence **110** or **101** is detected at its input. The sequences may overlap (i.e. input sequence 1101 must be detected twice). Operation and type of FSM can be determined from a given test sequence, where  $t_0 \dots t_{12}$  denote active edge transitions of clock signal  $CLK$ :

$CLK$	$t_0$	$t_1$	$t_2$	$t_3$	$t_4$	$t_5$	$t_6$	$t_7$	$t_8$	$t_9$	$t_{10}$	$t_{11}$	$t_{12}$
$w$	0	1	1	0	1	1	0	1	1	1	0	0	0
$z$	—	0	0	1	1	0	1	1	0	0	1	0	0

Examination duration is 60 minutes. Each assignment is worth 10 points.

Please sign your answer sheet using your enrollment number.

Solutions and examination results will be announced on course web page: <http://rds.fe.uni-lj.si>



Upon mistake cross the erroneous schematic and use the other one!

